

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:)	Group Art Unit: 2827
Michael John Watson)	
Serial Number 09/954,528)	F : 01 11
Filed: September 17, 2001)	Examiner: Chambliss
Title: IMPROVED ADHESIVES FOR)	
SEMICONDUCTOR APPLICA- TIONS EFFICIENT PROCESSES) S)	
FOR PRODUCING SUCH)	AMENDMENTS TO
DEVICES AND THE DEVICE)	THE SPECIFICATION
PER SE PRODUCED BY THE)	
EFFICIENT PROCESSES)	
)	
Attorney Docket: DC – 4952)	April 28, 2003

Assistant Commissioner For Patents Washington DC 20231

Dear Sir:

Please find attached a new page 7 with amendments at lines 10, 14, and 18, wherein the number "6" was substituted by the number -4 --.

Please also find enclosed page 1 of the specification wherein the title is amended.

Respectfully submitted,

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[0035] In Figure 10, there is shown yet another device package 11 of this invention that can be manufactured by the use of the adhesive of this invention in which there is shown a full side view of another device package 11 in which one semiconductor die 12 has been stacked on the top of the semiconductor die 2 to form said package 11.

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[0036] Thus, there is shown the circuitry substrate 3 which can be flexible or rigid, the die attach adhesive 5, containing the spacer beads 4 between the die 2 and the substrate 3, along with lead bonds 6, the solder balls 9, and another layer of die attach adhesive 13. The die attach adhesive 13 contains spacer beads 14, which for purposes of illustration of an embodiment of this invention said spacer beads 14 are smaller in size than the spacer beads 4 of the die attach adhesive 5. It should be noted by those skilled in the art that the average size of the spacer beads (particles) can be different between the different levels, or can be essentially the same, depending on the need of the manufacturer.

[0037] Assembly of such a device 11 is done by applying the adhesive 5 that contains the spacer beads 4, to the circuit board 15, that has been previously surmounted by the substrate circuit 3. Then, the hot die 2 is placed on the adhesive 5 with enough force to spread the adhesive 5 uniformly under the die 2. High pressures are not needed as can be observed by reviewing the viscosity of the die attach adhesive of the examples.

[0038] The heat partially cures the die attach adhesive 5 and the spacer beads 4 to provide a mechanism to control the height of the die 2 from the surface of the substrate 3.

Another die 12 can then be added on top of the previously mounted die 2 by applying adhesive 13 on top of the first die 2. The top die 12 is placed hot on the adhesive 13, allowing it to partially cure to hold the parts in place for subsequent wires 6 to be furnished in the bonding operations leading from the die 12 to the substrate. Full cure of the die attach adhesives 5 and 13 is completed when an overmolding is done on top of the package 11. Once an overmolding is applied and cured, solder balls 9 are added to complete the packaging of the package 11.

[0039] In the following examples, the die attach adhesive compositions of this invention are illustrated in more detail in which, unless otherwise specified, all parts and percentages are by weight. The examples are presented to further illustrate the invention and are not to be considered as limiting the invention in any way.



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DIE ATTACH ADHESIVES FOR SEMICONDUCTOR APPLICATIONS UTILIZING A POLYMERIC BASE MATERIAL WITH INORGANIC INSULATOR PARTICLES OF VARIOUS SIZES

[001] The invention disclosed herein deals with die attach adhesives and methods for their use, along with the devices that are obtained by the use of the methods.

[002] Using semiconductor chips as an example, the adhesives and the method for using them provides an interface between a chip (die) and the chip support. The method includes creating a space between the chip and the chip support of a given sized opening.

[003] BACKGROUND OF THE INVENTION

[004] In the construction of semiconductor assemblies, it has been found that curable elastomeric materials can be used to create a space between the semiconductor and its support, such construction being disclosed in the U.S. Patents of the prior art discussed *infra*. The most common is the assembly of one or more semiconductor chips on a substrate such as polyimide film which forms part of a chip carrier package including a circuit panel or chip housing.

[005] A chip carrier includes a dielectric layer with an array of terminals and may also contain leads. The chip carrier is fastened to a semiconductor chip through the leads or wire bonds. An elastomeric material is disposed between the chip and the flexible dielectric layer of the chip carrier. The chip carrier and elastomeric material are also referred to as an "interposer" or "interposer layer", by those skilled in the art. The leads or wire bonds of the chip carrier are bonded to the chip so that the terminals of the carrier are electrically connected to the contacts on the chip. The entire structure can then be mounted to a substrate such as a circuit panel or chip housing. The terminals of the chip carrier are electrically connected to contacts on the substrate. The elastomeric layer provides resiliency to the individual terminals allowing each terminal to move as necessary to accommodate tolerances during testing and in the final assembly itself.